WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor layer 1 of a first conductivity type having first and second major surface;

a second semiconductor layer 3 of a second conductivity type formed on the first major surface of said first semiconductor layer;

a third semiconductor layer 4 of the second conductivity type formed on said second semiconductor layer;

a fourth semiconductor layer 5 of the first conductivity type formed on said third semiconductor layer;

a first trench and at least one second trench 7, 11 arranged to penetrate through at least said fourth semiconductor layer from a surface of said fourth semiconductor layer;

a first semiconductor region 6 of the second conductivity type selectively formed in said surface of said fourth semiconductor layer adjacently to said first trench;

a first insulating film 8 formed on an internal wall of said first trench;

a control electrode 9 buried in said first trench through said first insulating film, said control electrode being not formed in said at least one second trench;

a first main electrode 12 electrically connected to at least a part of said first semiconductor region and formed over an almost whole surface of said fourth semiconductor layer; and

a second main electrode 13 formed on the second major surface of said first semiconductor layer.

2. The semiconductor device according to claim 1, wherein

a distance between said first trench and said at least one second trench is set to 5 μm or less.

3. The semiconductor device according to claim 1, wherein

said first trench includes a trench formed in a predetermined direction seen on a plane,

said at least one second trench includes a trench formed in said predetermined direction seen on a plane,

said first semiconductor region includes a first partial region formed in the vicinity of said first trench and a second partial region 6a to 6c extended from said first partial region in such a direction as to go away from said first trench; and

said first main electrode is directly formed on said second partial region to carry out electrical connection to said first semiconductor region.

4. The semiconductor device according to claim 3, wherein

said first semiconductor region includes a third partial region 6b, 6c which is further extended from said second partial region and is formed in the vicinity of said at least one second trench, and

said first main electrode is further formed directly on said third partial region to carry out electrical connection to said first semiconductor region.

5. The semiconductor device according to claim 4, wherein said second and third partial regions include a plurality of second and third partial regions respectively, and

said plurality of third partial regions 6c are selectively formed in the vicinity of said at least one second trench.

6. The semiconductor device according to claim 1, further comprising:

a second semiconductor region 16 of the first conductivity type formed in said surface of said fourth semiconductor layer adjacently to said at least one second trench, said second semiconductor region having a concentration of an impurity of the first conductivity type set to be higher than that of said fourth semiconductor layer.

7. The semiconductor device according to claim 6, wherein

said concentration of said impurity of the first conductivity type in said second semiconductor region is set to be higher than a concentration of an impurity of the second conductivity type in said first semiconductor region.

8. The semiconductor device according to claim 1, wherein

said at least one second trench includes a plurality of second trenches.

9. The semiconductor device according to claim 1, wherein

said first trench and said at least one second trench have equal formation widths.

10. The semiconductor device according to claim 1, further comprising:

a second insulating film 14 formed on an internal wall of said at least one second trench.

11. The semiconductor device according to claim 10, further comprising is a conductive region 15 buried in said at least one second trench through said second insulating film.

12. The semiconductor device according to claim 11, wherein

said first main electrode is directly formed on said conductive region.

13. The semiconductor device according to claim 1, further comprising:

a sixth semiconductor layer 2 of the second conductivity type formed between said first semiconductor layer and said second semiconductor layer, said sixth semiconductor layer having a concentration of an impurity of the second conductivity type set to be higher than that of said second semiconductor layer.

14. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a substrate including a first semiconductor layer 1 of a first conductivity type having first and second major surfaces and a second semiconductor

layer 3 of a second conductivity type formed on the first major surface of said first semiconductor layer;

(b) forming a third semiconductor layer 4 of the second conductivity type on said second semiconductor layer;

(c) forming a fourth semiconductor layer 5 of the first conductivity type on said third semiconductor layer;

(d) selectively forming a first semiconductor region 6 of the second conductivity type in a surface of said fourth semiconductor layer;

(e) selectively forming a first trench 7 to penetrate through at least said first semiconductor region and said fourth semiconductor layer from said surface of said fourth semiconductor layer;

(f) forming a first insulating film 8 on an internal wall of said first trench;

(g) burying a control electrode 9 in said first trench through said first insulating film;

(h) forming at least one second trench 11 adjacently to and apart from said first trench to penetrate through at least said fourth semiconductor layer from said surface of said fourth semiconductor layer;

(i) forming a first main electrode 12 electrically connected to at least a part of said first semiconductor region over an almost whole surface of said fourth semiconductor layer; and

(j) forming a second main electrode 13 on the second major surface of said first semiconductor layer.

15. The method of manufacturing a semiconductor device according to claim 14, wherein

said steps (e) and (h) are executed such that a distance between said first trench

and said at least one second trench is set to 5 μm or less.

16. The method of manufacturing a semiconductor device according to claim 14, wherein

said step (e) includes the step of forming said first trench in a predetermined direction seen on a plane,

said step (h) includes the step of forming said at least one second trench in said predetermined direction seen on a plane,

after said steps (d) and (e) are executed, said first semiconductor region includes a first partial region formed in the vicinity of said first trench and a second partial region 6a to 6c extended from said first partial region in such a direction as to go away from said first trench; and

said step (i) includes the step of directly forming said first main electrode on said second partial region.

17. The method of manufacturing a semiconductor device according to claim 14, further comprising the step of:

(k) forming a second semiconductor region 16 of the first conductivity type in said surface of said fourth semiconductor layer, said second semiconductor region having a concentration of an impurity of the first conductivity type set to be higher than said fourth semiconductor layer.

18. The method of manufacturing a semiconductor device according to claim 14, wherein

said step (e) and said step (h) are executed simultaneously.

19. The method of manufacturing a semiconductor device according to claim 14, further comprising the step of:

(l) forming a second insulating film 14 on an internal wall of said at least one

second trench,

said step (f) and said step (l) being executed simultaneously.

20. The method of manufacturing a semiconductor device according to claim 19, further comprising the step of:

(m) burying a conductive region 15 in said at least one second trench through said second insulating film,

said step (g) and said step (m) being executed simultaneously.